REMARKS

Introduction

Claims 1-127 were pending in this application.

Applicants have amended claim 40 to more particularly define the invention. Applicants have amended claims 123-127 to correct minor clerical errors. Applicants have cancelled claim 41 without prejudice. No new matter has been added and the amendments are fully supported and justified by the specification.

Reconsideration of this application in light of the following remarks is hereby respectfully requested.

Summary of the Office Action

Claims 1-101 and 122-127 are rejected under 35 U.S.C. § 102(e) as being anticipated by Sankey et al., U.S. Patent No. 6,400,291 (hereinafter "Sankey").

Claims 102-121 are rejected under 35 U.S.C. § 102(e) as being anticipated by Page et al., U.S. Patent No. 6,223,089 (hereinafter "Page").

Applicant's Reply to the Rejection of Claims 1-25 under 35 U.S.C. § 102(e)

Claims 1-25 are rejected under 35 U.S.C. § 102(e) as being anticipated by Sankey. The Examiner's rejections are respectfully traversed.

Applicants' invention, as defined by independent claim 1, is directed toward an apparatus for receiving and processing a clock data recovery (CDR) signal. The apparatus contains a programmable logic device (PLD) and processing circuitry. The processing circuitry is at least partly controlled by the PLD circuitry.

Sankey refers to a multiple time domain serial-to-parallel converter. The serial-to-parallel converter uses combinational logic to coordinate the serial-to-parallel conversion. The serial-to-parallel converter also includes a CDR device which receives a CDR signal and outputs a serial data stream. However, the CDR device of Sankey does not include PLD circuitry and is not controlled by a PLD or even by the combinational logic.

The Examiner asserts that the combinational logic of Sankey is the same as PLD circuitry and that this combinational logic at least partially controls the processing of the CDR device. Applicants respectfully disagree with the Examiner's assertion.

The combinational logic in Sankey does not control or even interface with the CDR device. Referring to FIG. 4 of Sankey, CDR device 94 receives a serial data stream 100 and a clock signal 120, but is not at least partially controlled by combinational logic 106. Thus, Sankey fails to

show "processing circuitry at least partially controlled by the PLD circuitry" as required by applicants' independent claim 1.

Accordingly, for at least this reason, applicants respectfully request that the rejection of claim 1 under 35 U.S.C. § 102(e) be withdrawn.

Claims 2-25 are dependent from claim 1 and are allowable at least because claim 1 is allowable.

Applicants' Reply to the Rejection of
Claims 26-39 and 71-101 under 35 U.S.C. § 102(e)

Claims 26-39 and 71-101 are rejected under 35 U.S.C. § 102(e) as being anticipated by Sankey. The Examiner's rejections are respectfully traversed.

Applicants' invention, as defined by independent claim 26, is directed toward an apparatus for producing and transmitting a CDR signal. Applicants' invention, as defined by independent claim 71, is directed toward an apparatus for transmitting an information signal which includes data information having clock information for the data information embedded in the data information.

The Examiner asserts that applicants' independent claims 26 and 71 are anticipated by Sankey. Sankey refers to an apparatus for receiving signals containing embedded clock information, however Sankey does not show an apparatus for

transmitting signals containing embedded clock information, as required by applicants' amended claims. Thus, Sankey fails to show the features of applicants' invention as defined by independent claims 26 and 71.

Accordingly, for at least this reason, applicants respectfully request that the rejection of claim 26 and 71 under 35 U.S.C. § 102(e) be withdrawn.

Claims 27-39 are dependent from claim 26 and are allowable at least because claim 26 is allowable. Claims 72-101 are dependent from claim 71 and are allowable at least because claim 71 is allowable.

Applicant's Reply to the Rejection of
Claims 40-70 under 35 U.S.C. § 102(e)

Claims 40-70 are rejected under 35 U.S.C. § 102(e) as being anticipated by Sankey. The Examiner's rejections are respectfully traversed.

Applicants' invention, as defined by amended independent claim 40, is directed toward an apparatus for receiving an information signal which includes data information having clock information for the data information embedded in the data information. The apparatus is configured to receive the information signal and a reference clock signal. The reference clock signal is related to the

frequency of the clock information embedded in the data information by a programmable scale factor.

The Examiner asserts that "Sankey inherently teaches [the reference frequency] to be programmable with respect to a scale factor." Office Action, page 7. Applicants respectfully disagree with the Examiner's assertion and wish to point out that when a reference is silent about an asserted inherent characteristic, evidence is required to show that the missing descriptive matter is necessarily present. See Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 1268 (Fed. Cir. 1991). The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. See In re Rijckaert, 9 F.3d 1531, 1534 (Fed. Cir. 1993). Applicants respectfully submit that the Examiner has failed to provide any evidence with respect the assertion that Sankey shows a reference clock signal having programmable scale factor. Sankey refers to a reference clock signal having a frequency related to the incoming serial data signal, but does not show or suggest a programmable scale factor relating the two frequencies. Thus, Sankey fails to show the features of applicants' invention as defined by amended independent claim 40.

Accordingly, for at least this reason, applicants respectfully request that the rejection of claim 40 under 35 U.S.C. § 102(e) be withdrawn.

Claims 41-70 are dependent from claim 40 and are allowable at least because claim 40 is allowable.

Applicants' Reply to the Rejection of
Claims 102-111 under 35 U.S.C. § 102(e)

Claims 102-111 are rejected under 35 U.S.C. § 102(e) as being anticipated by Page. The Examiner's rejections are respectfully traversed.

Applicants' invention, as defined by independent claim 102, is directed toward programmable serializer circuitry. The programmable serializer circuitry has input circuitry that receives a programmable number of input signals in parallel.

Page refers to a method and apparatus for enabling an operator terminal to remotely control a computer system. The method and apparatus includes transmission circuitry which contains a transmission link serializer. The serializer can only accept 16 or 20 bit words at a time.

The Examiner asserts that Page refers to programmable serializer circuitry that receives a programmable number of input signals in parallel. Applicants respectfully disagree with the Examiner's assertion.

Page refers to a serializer that "can only accept 16 or 20 bit words at a time." Page, column 5, lines 34-35. The serializer referred to by Page is not programmable to select between 16 and 20 bit word input modes nor is it programmable to receive words of any other size. Thus, the serializer of Page is not programmable to receive a programmable number of input signals in parallel as required by applicants' independent claim. Thus, Page fails to show the features of applicants' invention.

Accordingly, for at least this reason, applicants respectfully request that the rejection of claim 102 under 35 U.S.C. § 102(e) be withdrawn.

Claims 103-111 are dependent from claim 102 and are allowable at least because claim 102 is allowable.

Applicants' Reply to the Rejection of
Claims 112-121 under 35 U.S.C. § 102(e)

Claims 112-121 are rejected under 35 U.S.C. § 102(e) as being anticipated by Page. The Examiner's rejections are respectfully traversed.

Applicants' invention, as defined by independent claim 112, is directed toward programmable deserializer circuitry. The programmable deserializer circuitry receives an input signal that is serially indicative of plural bits of

information one after another and stores a programmable number of successive ones of those bits.

Page refers to a deserializer which receives serial data and outputs the data as 14 bit wide parallel words.

The Examiner asserts that Page refers to a programmable deserializer circuitry that receives and stores a programmable number of successive bits. Applicants respectfully disagree with the Examiner's assertion.

The deserializer referred to by Page stores and outputs parallel words having 14 bits. Accordingly, the deserializer of Page does not store a programmable number of successive bits to output as parallel words, as required by applicants' independent claim. Thus, Page fails to show the features of applicants' invention.

Accordingly, for at least this reason, applicants respectfully request that the rejection of claim 112 under 35 U.S.C. § 102(e) be withdrawn.

Claims 113-121 are dependent from claim 112 and are allowable at least because claim 112 is allowable.

Applicants' Reply to the Rejection of
Claims 122-127 under 35 U.S.C. § 102(e)

Claims 122-127 are rejected under 35 U.S.C. § 102(e) as being anticipated by Sankey. The Examiner's rejections are respectfully traversed.

Applicants' invention, as defined by independent claim 122 relates to an apparatus for receiving and processing a plurality of CDR signals, each CDR signal having data and clock information. The apparatus contains a first circuitry and a plurality of second circuitries. The first circuitry produces a plurality of candidate recovered clock signals having phases that are shifted relative to one another. The second circuitries each receive a respective one of the CDR signals and use the candidate reference clock signals to recover the clock information from the CDR signals.

The Examiner asserts that Sankey shows all of the elements of applicants' claim 122. Applicants respectfully disagree with the Examiner's contention. Sankey refers to multiple serial-to-parallel converters 96, each serial-to-parallel converter 96 is connected to a CDR circuit 94. CDR circuit 94 receives a CDR signal 100 and an alignment clock 120. However, Sankey does not show a plurality of CDR circuits 94 all connected to alignment clock 120. Thus, Sankey does not show or suggest connecting a plurality of candidate recovered clock signals to a plurality of CDR circuits as required by applicants' independent claim 122.

Accordingly, for at least this reason, applicants respectfully request that the rejection of claim 122 under 35 U.S.C. § 102(e) be withdrawn.

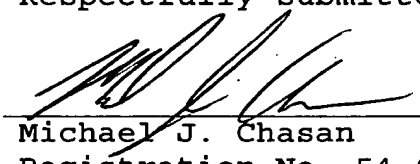
Claims 123-127 are dependent from claim 122 and are allowable at least because claim 122 is allowable.

Conclusion

For at least the foregoing reasons, applicants respectfully submit that this application is in condition for allowance.

Accordingly, prompt reconsideration and allowance of this application are respectfully requested.

Respectfully submitted,



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